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Radiation induced soft errors in 16 nm floating gate SLC NAND flash memory

Sandhya Chandrashekhar[a,*], Helmut Puchner[a], Jun Mitani[a], Satoshi Shinozaki[b], Mohamed Sardi[b], David Hoffman[a]

[a] Cypress Semiconductor Corporation, United States of America
[b] SkyHigh Memory Limited, Hong Kong

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ABSTRACT

16nm single-level-cell (SLC) NAND flash memories with 1-bit ECC are shown to have excellent robustness to soft errors induced by terrestrial neutron radiation and alpha particles. Accelerated stress test studies were done at TRIUMF Neutron Facility for neutron induced soft errors and using calibrated alpha sources for accelerated alpha particle testing. Our results demonstrate excellent robustness of the memory device to soft error latch-up and single event upsets. Additionally, we report cross-site correlation results of accelerated alpha particle testing of 16nm NAND flash memories by comparing test results using Am-241 and Th-232 foils for higher confidence in the failure rate calculations. An acceleration factor of 1.66×10^4 between the two foils was used.

1. Introduction

Space and aerospace applications increasingly require high-capacity, high-speed, compact mass nonvolatile memories. The chief barrier to adoption of "COTS" – which stands for commercial off-the-shelf devices for Military and space applications – is the radiation threat to the active electronic components [1–3]. Radiation induced errors is also a concern in certain medical applications where electronics are subjected to sterilization by irradiation or exposed to high radiation therapy environments. This threat is particularly high for highly scaled devices manufactured in the sub-20 nm technology nodes which have altogether fewer electrons available in the charge storage node [4,5]. The critical charge parameter or Q_{crit} (product of capacitance of a node and voltage across it) is the minimum electron charge disturbance needed to disrupt the logic state. Reduction in chip feature size and supply bias in scaled devices decreases Q_{crit} and renders it more susceptible to failures.

Terrestrial neutron radiation result from collision of cosmic rays with atmospheric atoms typically nitrogen and oxygen and less than 1% reach the sea level with energy spectrum exhibiting three peaks corresponding to thermal neutrons (0.01 MeV–0.2 MeV), spallation (0.1 MeV–5 MeV) and high energy neutrons (10 MeV–1000 MeV) [1]. Neutron flux is sensitive to altitude and peaks at the Earth's poles. Solar winds and solar flares also contribute to the neutron flux in Earth's atmosphere. Neutrons are uncharged but may have sufficient energy to be captured by atomic nuclei resulting in secondary ionizing particles that can cause soft errors. Studies have shown that energetic neutrons form 95% of the particles capable of causing soft errors with the rest being attributed to protons and pions [6–8]. Most studies are focused on neutron radiation induced errors, but there are also recent publications on proton induced soft errors in circuits [9]. All matter surrounding us also contains trace radioactive impurities like ^{210}Po, ^{238}U, and ^{232}Th. In semiconductor components, these isotopes are typically found contaminating the mold compound and the solder material [10]. These radioactive isotopes with short half-lives spontaneously decay into more stable forms by emitting alpha particles which are doubly charged Helium ions (He^{2+}). They are strongly ionizing particles capable of generating enough several electron-hole pairs in silicon to disrupt the state of the circuit, forward bias junction nodes and/or discharge storage nodes and alter the bit state of the memories resulting in bitflips. High-density devices lend themselves to high risk of errors [11]. The errors caused by radiation are generally considered soft since they do not damage or alter the physical properties of the circuit, device or atoms and the system typically recovers by reprogramming the part with correct data set or a reset power-cycle. Single event effects (SEE) in Flash memories are related to Single event upset (SEU), Multi-bit upset (MBU) and Single event latch-up (SEL) [6,12]. These events are random, and observation of a soft error does not indicate that the

* Corresponding author.
E-mail addresses: Sandhya.Chandrashekhar@cypress.com, sanc@cypress.com (S. Chandrashekhar).

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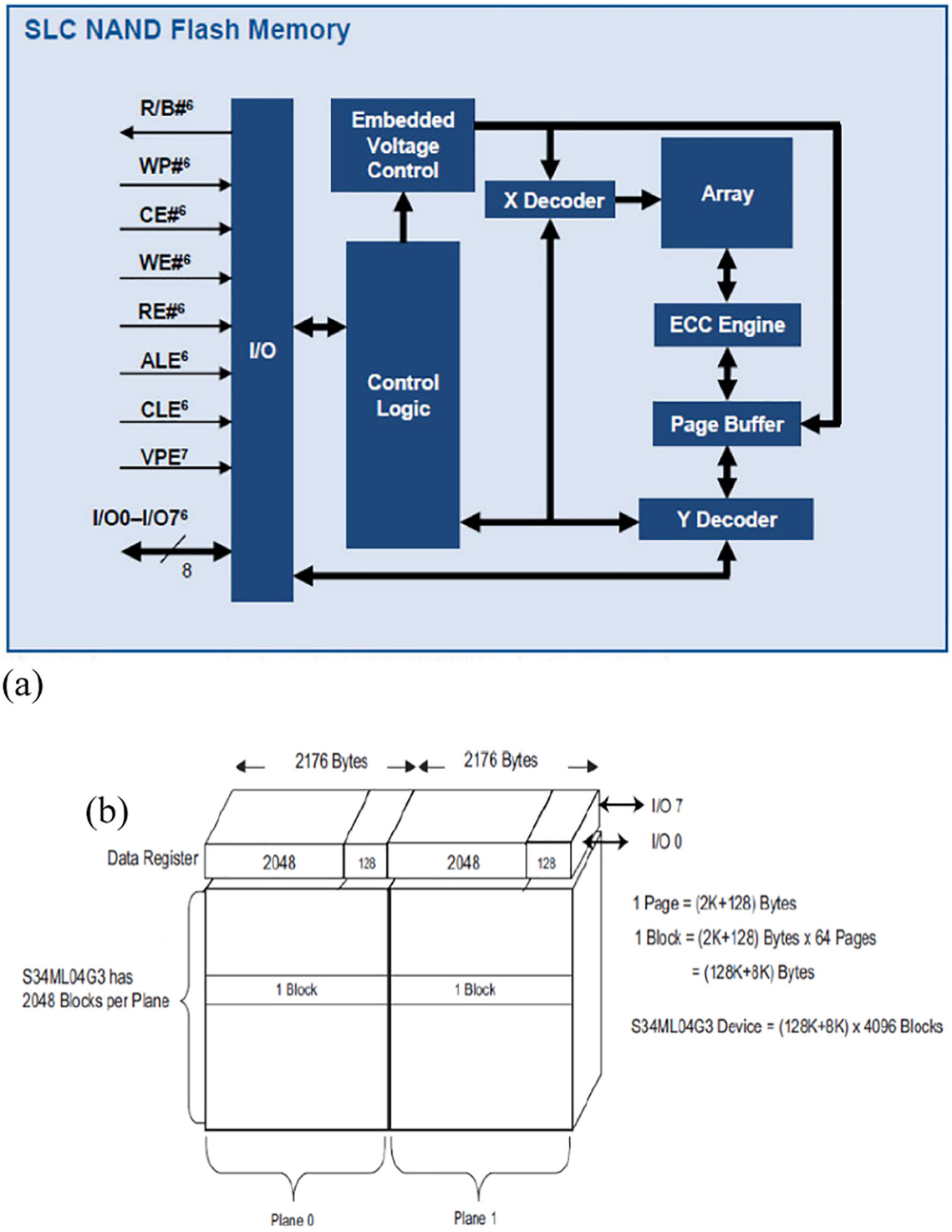

Fig. 1. (a) The 4Gb Flash block diagram. (b) Flash array organization.

system reliability is any less than before. Highly reliable systems use error detection and correction schemes, fault tolerant design and built in system redundancies to cope with soft errors on the fly. In flash memories, error correction code (ECC) algorithms are very effective in protecting the memory from soft errors, but they add to the cost, latency and the size of the chip [1]. In addition, critical device failures may occur when the number of bit errors exceeds the limit correctable by the embedded ECC algorithm.

This paper discusses the soft error effects of a 4 Gb Single Level Cell (SLC) Floating gate NAND Flash memory product fabricated on a planar 16nm technology for embedded applications. This non-volatile memory is Open NAND Flash Interface (ONFI) 1.0 compliant with address, data, and commands multiplexed. This memory device also includes a one-time programmable (OTP) area consisting of one block or 64 pages. OTP area has restricted access where sensitive data/code can be stored permanently. ECC algorithms add redundancy to the data to improve the overall reliability of the system. Since it is intended for automotive applications, the SLC NAND flash product embeds a robust 1-bit ECC support. Fig. 1a shows the block diagram of the memory architecture. The non-volatile flash memory is offered with a 3.3V nominal power

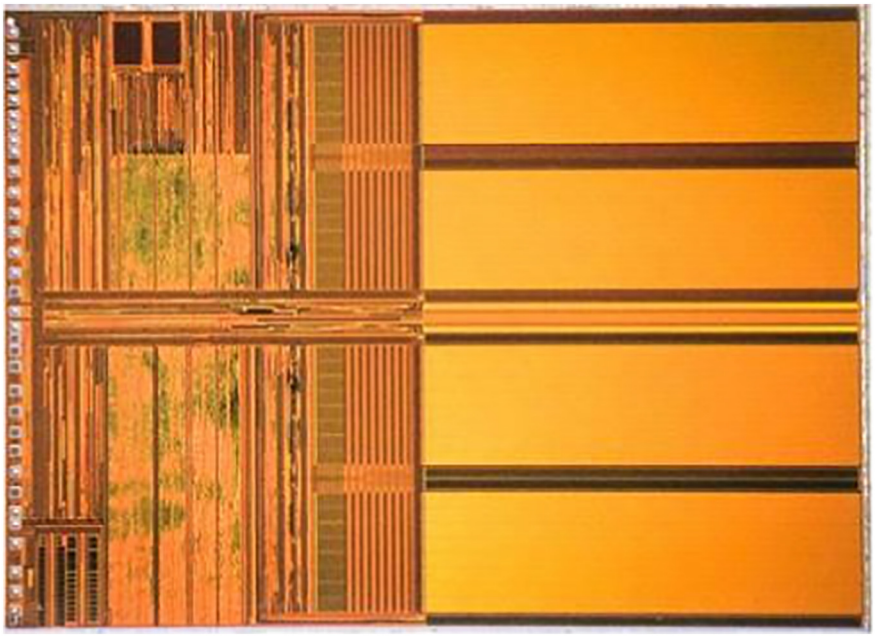

Fig. 2. Top-view image of the die.

supply voltage, and ×8 I/O interface. The on-chip Program/Erase Controller automates all read, program, and erase operations including pulse repetition, internal verification and margining of data. Commands, Data, and Addresses are asynchronously introduced using CE#, WE#, ALE, and CLE control pins. The WP# pin provides hardware write protection against undesired program and erase. The Ready/Busy (R/B#) output pin signals the status of the device during each operation to identify if the program/erase/read controller is currently active.

A detailed schematic of the array organization is depicted in Fig. 1b. There are two memory planes with 2048 blocks divided into 64 pages with 2048 bytes and 128-byte spare area. Since the blocks can be erased independently, it is possible to preserve valid data while old data is erased. The program operation typically writes 2 KB page in 350 μs and an erase operation typically completes in 4.0 ms on a 128-KB block.

Fig. 2 shows the image of the die photographed from the top having size of 4.34 mm × 5.14 mm. A 48-pin Thin Small Outline Package (TSOP) with dimension of 18.4 × 12.0 × 1.2 mm was used for the radiation sensitivity tests.

This flash memory is qualified for industrial and automotive applications and is expected to operate from −40 °C to 85 °C Industrial grade operational temperature range and from 105°C Industrial-Plus temperature range. It is intended for mission critical applications like automotive cluster and infotainment systems, industrial control and automation, networking, server equipment, and commercial applications like consumer electronics. While ECC ensures that the NAND flash is protected against single bit errors, failures due to multi-bit errors or single event latches (for example, localized micro-latches in the decoder circuitry) may not have adequate immunity to radiation-induced errors. Hence, it is important to understand the data corruption susceptibility of the memory array due to terrestrial cosmic radiation and potential contamination in package due to radioactive impurities [11]. In this work, the neutron and alpha induced SER contributions have been separately characterized to provide the complete assessment of the product's soft error sensitivity.

2. Materials and methods

This section describes the stress test method used for accelerated neutron and alpha irradiation testing. The test conditions and configurations for testing SEL and SEU are provided and the results are discussed in the following section.

2.1. Neutron irradiation stress testing method

The accelerated studies with neutron radiation testing was conducted at the TRIUMF Neutron Facility (TNF) which has a neutron beam spectrum comparable to the high energy terrestrial neutron spectrum at the reference sea-level New York City (NYC) location [13]. Logical checkerboard (CKBD) pattern was programmed on the Devices Under Test (DUTs) at room (25 °C) and hot (85 °C) conditions through ATE. The DUTs were then placed in an antistatic carrier tray and lowered into the neutron beam located 16 ft below floor level of the TNF facility at room temperature for determining the chip SER. The devices are unbiased during the test. Read verification post stress was done to compute stress-induced bit error rate (BER) and Failure in Time (FIT) failure rate computed. For the SEL testing, each DUT was soldered to a carrier card with a DIP (Dual Inline Pattern) footprint. The DUT carrier card was then inserted into a socket on a test card and mounted on to a metal carrier plate. Fig. 3 shows the experimental apparatus mounted on the metal plate used for the test.

To raise the temperature of the DUT for evaluating latch-up, a heater strip and a temperature sensor were placed underneath the carrier card. The top surface temperature of the DUT was monitored using an IR thermometer and the heater's bias adjusted until the surface temperature was stable at ~105 °C. When the biased DUT reached target temperature, the metal plate was lowered into the neutron stream. Static SEL testing was performed with the all DUTs heated to temperature of 105 °C and maximum Vcc = 3.6 V. The duration of exposure of DUTs was planned to achieve a fluence that is statistically significant to achieve a low FIT rate. The neutron fluence was recorded by a detector located behind the carrier plate.

2.2. Alpha radiation stress testing method

Accelerated alpha radiation testing was conducted at our laboratories using two different alpha sources. The Thorium foils have a broad spectrum between 2 MeV and 9 MeV approximates the uranium and plutonium isotope alpha particle emission from the mold compound at highly accelerated conditions. However, Th-232 sources with sufficiently high flux are rare, causing test duration to be longer. Hence,

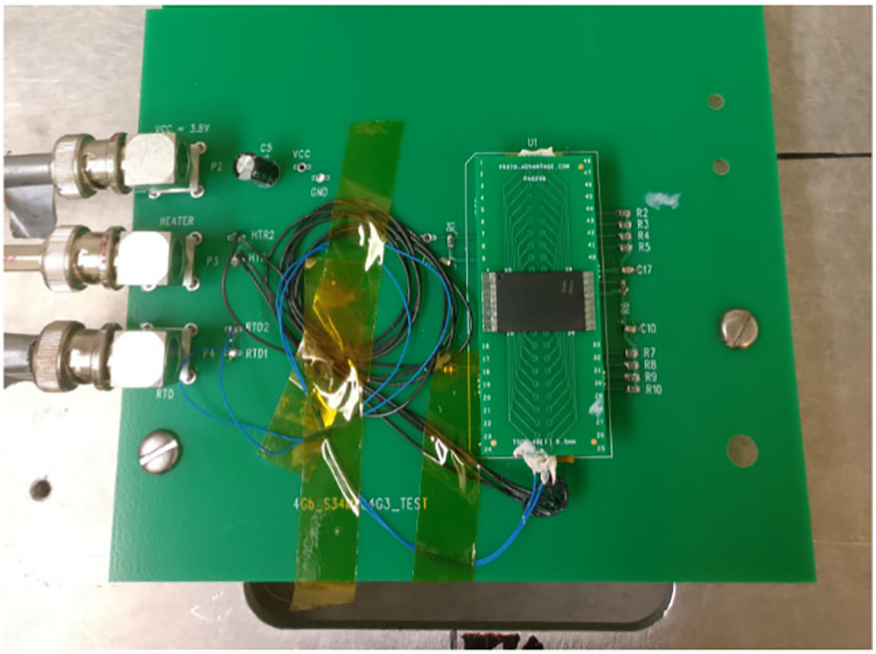

Fig. 3. Experimental setup for biased neutron SEL test.

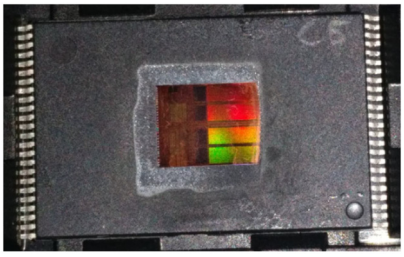

Fig. 4a. Decapsulated package with exposed die used for alpha radiation testing.

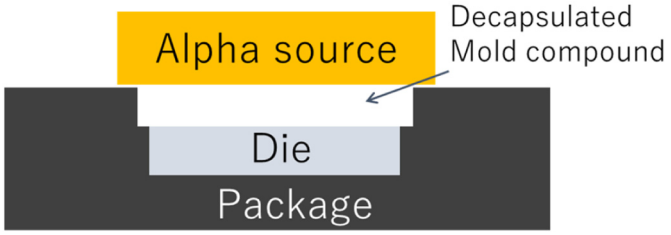

Fig. 4b. Schematic showing the alpha radiation test setup.

mono-energetic sources like Americium (Am-241) with peak at 5.4 MeV or Curium (Cm-244) with peak of 5.7 MeV are often used for highly accelerated testing especially for components with intrinsically super low FIT rates [1]. To correlate the results from alpha sources with different energy spectrum, tests were run using Th-232 at San Jose, CA, USA and Am-241 at Kawasaki, Japan. The Th-232 foil was certified to have alpha emission rate of 4798 alpha/cm^2 min while the Am-241 foil certified as 3 MBq and known to have surface area of 1 cm^2. DUTs were first decapsulated as shown in Fig. 4a and then programmed with logical CKBD pattern with ECC turned on for one half memory plane and ECC turned off for the other half plane. The alpha source is then placed over the exposed, unbiased die as shown in Fig. 4b, at the two test sites. Location and altitude do not impact alpha radiation testing since they have the least penetrating power and can travel only a few centimeters in air before losing energy by scattering or being absorbed by matter.

3. Theory, results and discussion

This section describes the results obtained from the tests and the computation of the failure rate. FIT (Failure in Time) is commonly used to specify failure rates and is defined as number of failures expected every 10^9 h [6]. The threshold voltage (Vt) distributions before and after stress were generated by sampling a predefined number of memory blocks from top, center and bottom of the memory array.

3.1. Neutron radiation testing results and discussion

A summary of SEL results is shown in Table 1. Test was conducted with sample size of 3 units from a single wafer lot. The test duration extended until the target fluence was reached and neutron count was recorded. No arbitrary jumps or increase in standby current was observed at the output pin that was continuously monitored during the static SEL test. Package top surface temperature was measured using IR sensor before and after test to verify the DUT surface temperature of 105 °C.

The soft error failure rate induced by neutron accelerated test is normalized to the flux of 13 neutrons count/cm^2 h at reference NYC sea level and reported in FIT/Mbit for SEU and FIT/Device for SEL.

The SEL FIT rate computation follows Eq. (1).

$$FIT\left[\frac{1}{Dev}\right] = \frac{(\#LUevents)\cdot 10^9 \text{h}}{\Phi_{ACC}/\Phi_{NYC}} \quad (1)$$

where, LUevents = Number of latch-up events observed,
Φ_{ACC} = Flux from accelerated neutron source, and
Φ_{NYC} = Flux at NYC sea level.

Table 1
Summary of results from neutron SEL test.

DUT#	SEL test conditions			
	Temperature (°C)	Vcc (V)	$I_{standby}$ (mA)	Fluence (n/cm^2)
1	107.7	3.6	0.022	4.44×10^9
2	106.7	3.6	0.022	4.44×10^9
3	104.9	3.6	0.022	4.44×10^9

From the measured data, the point estimate of SEL failure rate was computed to be less than 2.7 FIT/device.

Neutrons are uncharged particles, but they can interact with the heavier atoms of Cu, W etc. that form the back-end metallization and vias to generate secondary reaction products which can impinge on the sensitive storage node and perturb the electronic charge stored in the floating gate [14]. The key charge loss mechanism however, is caused by a direct collision of the neutron particle inside the floating gate region resulting in a burst of charge (electron and hole pairs) as well as secondary spallation products (alpha particles, etc.). The spallation products are typically less of a concern since their energy level is reduced compared to the incoming neutron particle. The major charge loss now is from holes drifting from the collision site. Since the electrons have a higher drift mobility, they can quickly recombine with dangling bonds at the material interfaces, resulting in a net positive charge due to remaining holes that will reduce the Vt of a programmed cell.

The SEU test was conducted on a sample size of 3 units each from 3 different wafer lots with the DUTs unbiased and at room temperature. Post neutron irradiation, the 3 control units and the 9 exposed DUTs were read verified to evaluate bit integrity. Fig. 5 shows the comparison of the programmed bit Vt distributions before and after neutron irradiation. The erased bit distribution is mostly unchanged from particle exposure. Table 2 provides overview of the results from the neutron SEU test.

A maximum shift of 200 mV was observed with the programmed state being more sensitive to radiation than the erased state of which ~100 mV can be attributed to the intrinsic Vt shift averaged on the control units. It is to be noted that neutron fluence under test is equivalent to 40,000 years of exposure in field scaled to New York City sea level, which is significantly larger than the expected lifetime of the product in field usage condition. There were no bitflips observed post neutron irradiation in all DUTs tested indicating the robustness of the flash array to the radiation induced data corruption. Neutron SEU failure rate is computed as shown in Eq. (2):

$$FIT\left[\frac{1}{Mb}\right] = \frac{(\#errors)\cdot 10^9 h}{density\,[Mb]\cdot(\Phi_{ACC}/\Phi_{NYC})} \quad (2)$$

where, #errors = Number of bitflips observed,

Φ_{ACC} = Flux from accelerated neutron source, and

Φ_{NYC} = Flux at NYC sea level.

Based on the duration of exposure and the neutron fluence during test, the results indicate an average failure rate of 0.001 FIT/Mb for the 16 nm NAND flash memory indicating excellent immunity to high-energy neutron induced soft errors.

Table 2
Summary of results from neutron SEU test.

DUT#	SEU test conditions				
	Temperature (°C)	Pattern	Bitflips (#)	Fluence (n/cm^2)	FIT/Mb
1–3	25	CKBD	0	4.44×10^9	0.001
3–6	25	CKBD	0	4.44×10^9	0.001
6–9	25	CKBD	0	4.44×10^9	0.001

3.2. Alpha radiation testing results and discussion

The alpha radiation stress experiment also serves as an opportunity to compare the relative strengths and effectiveness of the two alpha sources. The charge loss mechanism due to alpha particle is similar to neutrons except that the charges are generated by coulombic interaction of the alpha particle with silicon while drifting through the floating gate. They are strongly ionizing particles capable of generating several electron-hole pairs in silicon. Again, the generated electrons recombine at the interface leaving behind a net positive charge which results in charge loss of the programmed cell. This has less impact on the erased cell since the erased floating gate contains almost no electrons and is not significantly perturbed by the positive charge.

Calibration of the two alpha sources was done by examining memory blocks programmed with ECC off to measure and evaluate the raw bit errors. The intent of turning ECC off is to study all modes of failure that can potentially occur in the flash array. This becomes important when the number of bit fails (single bit upsets and multi cell upsets) exceed the error correction capability of the ECC algorithm and creates risk of a fatal field failure. Note that in this experiment we verified that the embedded ECC can correct all possible bit errors and deliver a very robust memory array immune to alpha particle upsets.

Using Am-241 foil, tests were conducted on a total sample size of 9 units with 3 units each from 3 different fab lots. The parts exposed to Am-241 were exposed for maximum of 20 s, with intermediate readpoint at 10 s since the output flux of this source is known to be significantly higher than Th-232. Alpha radiation tests were conducted on a sample size of 3 units each from 3 different wafer lots for each stress duration when testing with Th-232 foil. The length of exposure duration was systematically increased in steps from 5 h to 65 h to study the tolerance of the product to alpha radiation. In both cases, 3 control units were read to subtract bitflips not caused by alpha exposure (but caused by other mechanisms such as data retention loss) from the readout of bitflips of stressed units. The Vt distributions were measured before and after final exposure for devices stressed using Th-232 (Fig. 6)

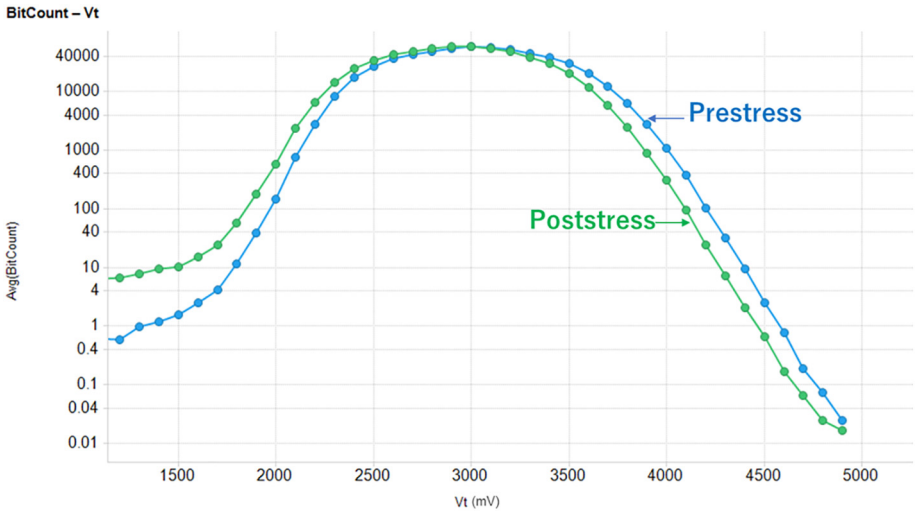

Fig. 5. Neutron average bit count program Vt distribution before and after neutron irradiation.

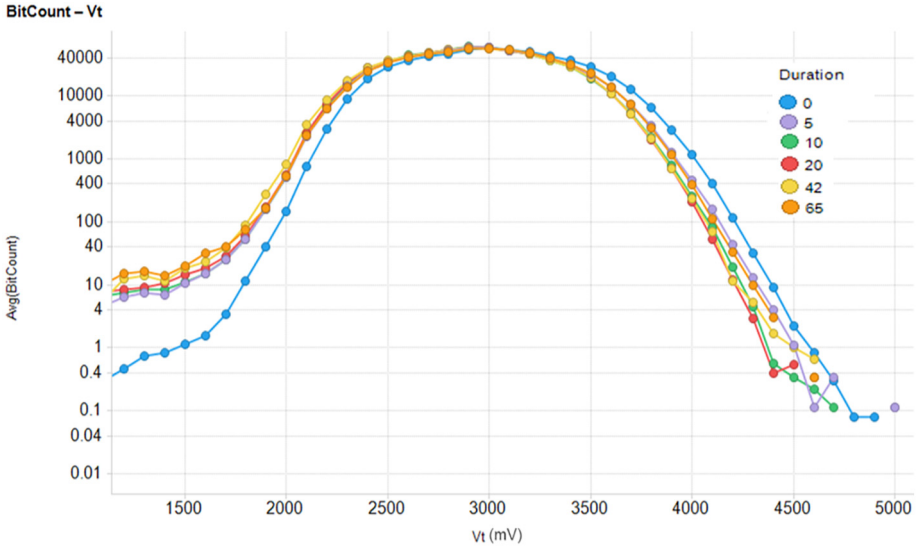

Fig. 6. Comparison of program Vt distribution before and after exposure to alpha particles from Th-232 source for progressively increasing exposure duration (in hours).

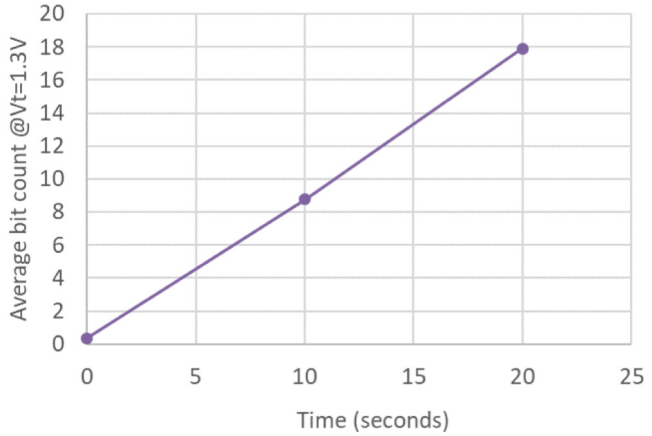

Fig. 7. Comparison of program Vt distribution before and after exposure to Am-241 alpha particles for progressively increasing exposure duration (in seconds).

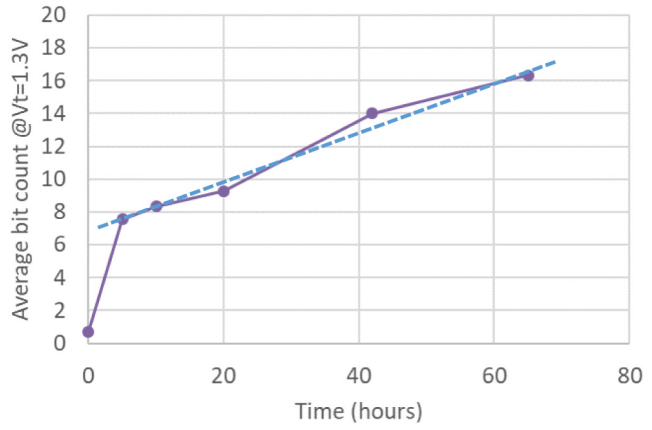

Fig. 8a. Linear increase in average bit count measured at reference program Vt after exposure to Am-241 alpha particles.

and Am-241 (Fig. 7). Overall, a 250 mV–400 mV shift in Vt distribution post-stress is observed which also includes a 100 mV averaged shift in the program bit distribution attributed to the intrinsic charge loss as measured on control units. The exposure to alpha particle spreads the tails of the lower program bit distribution, with the bits programmed to lower threshold voltages being most vulnerable. As expected, there is a near linear dependence of bit errors versus exposure duration as shown in Figs. 8a and 8b. The time scale of the measurement is in seconds for Am-241 exposure and hence readouts were made with minimum delay post stress test. With Th-232 however, the parts were programmed and shipped to the test site and then shipped again for read verification and hence the initial jump in Fig. 8b is mainly due to intrinsic charge loss.

Average bit error rate without embedded error correction code after alpha exposure is shown in Fig. 9 for Th-232 source and Fig. 10 for Am-241 source. Bit error rate (BER) is calculated from the following equation [14]:

$$\text{BER} = \text{Total number of bit errors/Total number of tested bits} \tag{3}$$

BER is often used as a parameter to analyze NAND flash memory read data. The purpose is to normalize read error by dividing total tested bits to facilitate comparison across memory devices with varying array densities. As observed in Figs. 9 and 10, the average BER linearly increases with alpha particle exposure duration. The devices subjected to stress with the calibrated Th-232 source exposure causes average BER to increases linearly with exposure duration with effective slope of 6.35×10^{-7} BER/h. BER with Am-241 source with slope of 1.05×10^{-2} BER/h suggests that the Am-241 source is significantly more active than Th-232 source. The ratio of slope can be considered as the acceleration factor between the two foils and is 1.66×10^{4}. Therefore, Am-241 foil alpha emission rate is 7.95×10^{7} alpha/cm^2/min, which is calculated by multiplying the acceleration factor with the calibrated Th-232 foil alpha emission rate of 4798 alpha/cm^2/min. The total test duration using Am-241 source was few seconds while the testing with Th-232 source lasted several hours and days.

The SEU failure rate is computed using Eq. (4) below:

$$FIT\left[\frac{1}{Mb}\right] = \frac{(\#errors)\cdot 10^{9} h}{density\,[Mb]\cdot(\Phi_{FOIL}/\Phi_{PKG})} \tag{4}$$

where, #errors = Number of bitflips observed,

Φ_{FOIL} = Accelerated flux from alpha source, and

Φ_{PKG} = Flux from the materials constituting the package.

The failure rate was computed to be 46 FIT/Mb using Eq. (4) when stress tested using Am-241, and for devices stressed using Th-232 foil was found to be 49 FIT/Mb — comparable but slightly higher than the failure rate independently obtained using the Am-241 source for the same device. Under accelerated conditions of this experiment, exposure

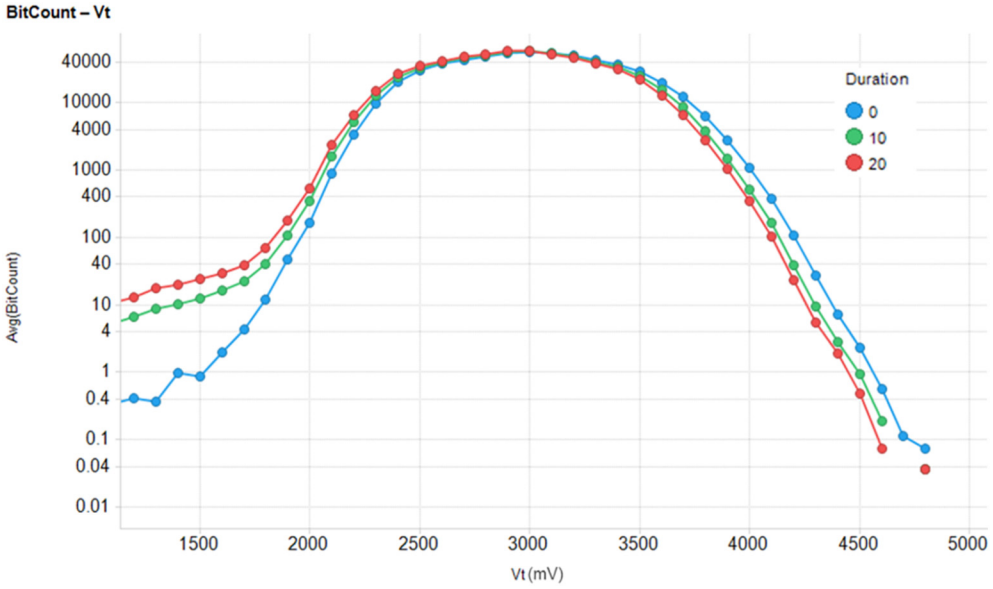

Fig. 8b. Near linear increase in average bit count measured at reference Vt after exposure to Th-232 alpha particles. The dotted line provides guide to the eye.

dose given to DUTs is equivalent to several thousand years under field use conditions. The overall stress acceleration is 1.44×10^9 over a standard mold compound emission rate of 0.02 alpha/cm^2 h. The lifetime is predicted to be longer with production grade packages using Ultra Low Alpha (ULA) mold compounds with emissivity of 0.001 alpha/cm^2 h. With ECC on, there were no bitflips observed post radiation from both sites and the effective failure rate is computed to be less than 0.0005 FIT/Mb. Thus, the embedded 1-bit ECC delivers a very reliable memory array immune to all alpha particle upsets by correcting all possible tail bits in this distribution.

4. Conclusion

In this work, we characterized 16 nm NAND Floating Gate Flash memory in a 48TSOP package for the soft error susceptibility. The overall soft error estimation was done by measuring neutron (SEL, SEU) and alpha radiation (SEU) effects separately. With the robust 1-bit ECC, no un-correctable data bit errors were observed demonstrating excellent immunity of the memory to soft errors in terrestrial environments on a scaled technology node. Further, the cross-site calibration experiment for alpha radiation testing served to qualify Am-241 as a calibrated source that can be used to achieve faster turn-around in SEU testing without compromising on the accuracy of the results.

Any observed bitflips due to particle exposure were localized on programmed cells only. No bitflip of any erased cell has been observed. Since advanced NAND memory cells suffer from transient data retention loss it is recommended to perform the pre-post distribution analysis and read/write verification immediately before and after radiation exposure. Preferably at the radiation test site to eliminate potential bitflips due to data retention charge loss. If pre-post testing cannot be accommodated at the radiation test site it is recommended to have a significant amount of non-radiated control units in parallel to subtract the bitflips related to the data retention charge loss.

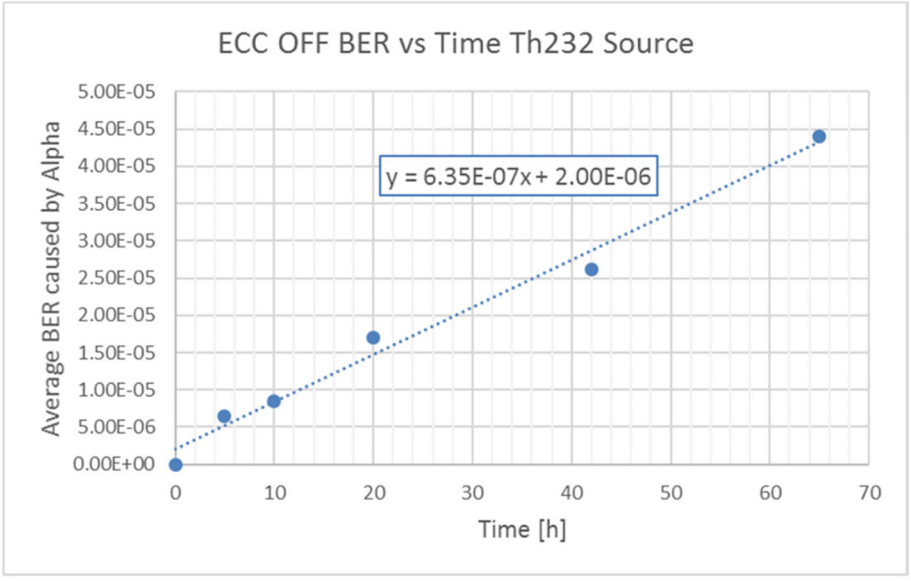

Fig. 9. Average bit error rate after Th232 alpha radiation exposure.

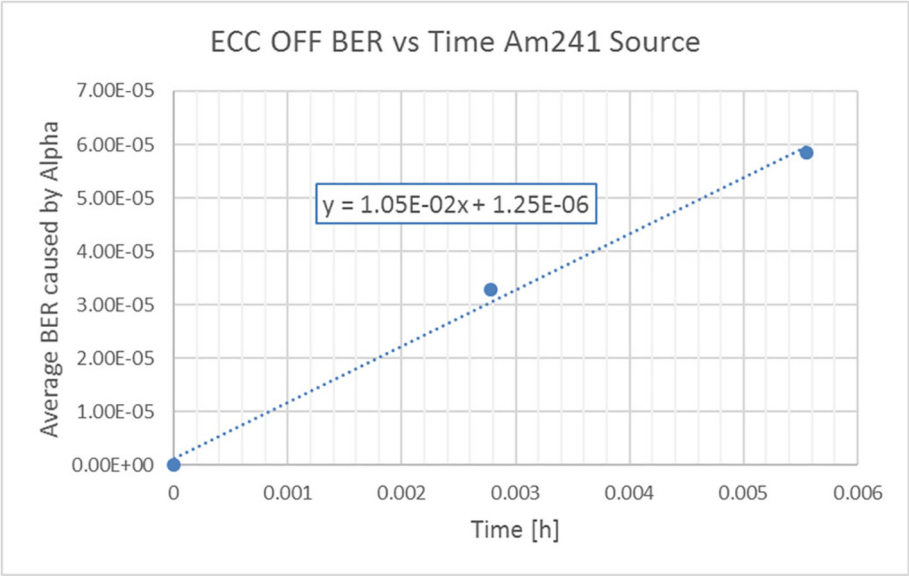

Fig. 10. Average bit error rate after Am241 alpha radiation exposure.

Declaration of competing interests

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

CRediT authorship contribution statement

Sandhya Chandrashekhar:Conceptualization, Methodology, Investigation, Formal analysis, Writing - original draft, Writing - review & editing.**Helmut Puchner**:Resources, Supervision, Writing - review & editing.**Jun Mitani**:Methodology, Investigation, Data curation, Formal analysis, Writing - review & editing.**Satoshi Shinozaki**:Data curation, Validation, Writing - review & editing.**Mohamed Sardi**:Funding acquisition, Project administration.**David Hoffman**:Project administration.

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