SLC Versus MLC NAND Flash Memory

AN200602 describes the differences between single-level cell (SLC) and multi-level cell (MLC) NAND flash memory.

1   Introduction

This application note describes the differences between single-level cell (SLC) and multi-level cell (MLC) NAND flash memory.

2   Flash Memory Basics

A flash memory cell consists of a single transistor with a floating gate that can store electrons. The number of electrons on the floating gate can alter the threshold voltage (V_t) of the transistor and this is what determines if the cell is programmed '0' or erased '1'.

Figure 1. Floating Gate Flash Transistor Cross-Section
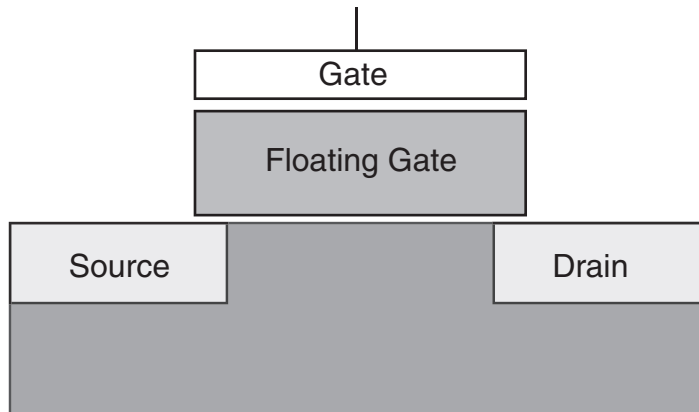
SLC flash memory is where a single physical cell can store one bit of data. It can have two states, '0' (programmed) or '1' (erased).

Figure 2. SLC V_t Distribution
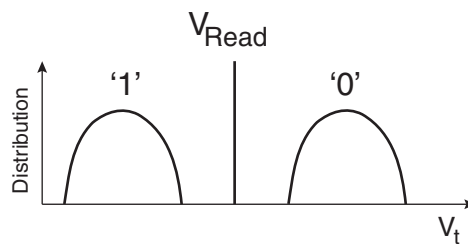
MLC flash memory is where a single physical cell can store two bits of data. It can have four states, '00' (programmed), '01' (partially programmed), '10' (partially erased), or '11' (erased). Programming for an MLC device needs to be carefully done so that the V_t is within the window for the desired state.

Figure 3. MLC V_t Distribution
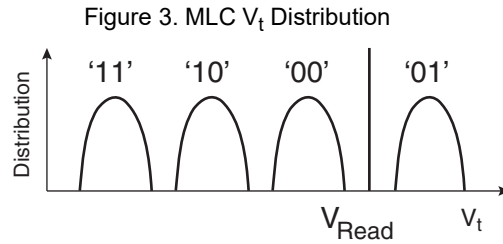
3 SLC vs MLC Specification Comparison

Table 1 is a comparison of key specifications between SLC and MLC NAND flash memory.

Table 1. Feature Comparison between SLC and MLC Devices.

Features	SLC	MLC
Bits per Cell	1	2
Voltage	3.3V, 1.8V	3.3V
Data Bus Width (Bits)	x8, x16	x8
Planes	1 or 2	2 or more
Page Size (Bytes)	2k	4k or more
Pages Per Block	64	128 or more
ECC (per 512 Bytes)	4-bit or more	12-bit or more
Program/Erase Cycles	100k	3k to 5k
Number of Partial Pages	4	1
Read	25 µs	50 to 60 µs
Program	200 µs	1100 to 1300 µs
Erase	2 ms	3 to 4 ms

Note:

1. *Based off of 3X and 2X technology nodes.*

Since MLC contains two bits of data per cell versus one bit of data per cell for SLC, it is easy to see that MLC has a distinct advantage in offering higher density products. Assuming the wafer size and process technology are the same, a MLC product will have about 2X the density of the SLC product.

SLC has a clear advantage in most other areas such as write performance, endurance, and lower error rates. Write performance is worse on the MLC device since it requires a more extensive programming algorithm. The algorithm needs to carefully store charge on the floating gate to get the V_t's within a tight window for the desired programming state.

SLC will have 10x better endurance as compared to a MLC device. Programming the flash cell can lead to damage in the oxide layer which could alter the V_t of the cell. This is true for both a SLC and MLC device. However, a MLC device has a much tighter window for the V_t placement, so any damage to the oxide layer will be felt earlier on the MLC device than the SLC device. Consequently, a SLC device is rated at a minimum of 100,000 program/erase cycle and a MLC device is rated at a minimum of 5,000 program/erase cycles.

SLC will have a lower Raw Bit Error Rate (RBER) than a MLC device. Leakage or disturbs could shift the V_t within the cell and lead to a read error. Due to the tight window of Vt placement for a MLC device, it is more susceptible to a read error. With a higher error rate for the MLC device, it will require a stronger ECC (Error Code Correction) to protect against read errors. The processor or controller will need to support the larger ECC algorithms. SLC would be a better choice for older processors which only support smaller ECC algorithms.

TLC is another type of NAND flash memory which stores three bits of data per physical cell. This will allow the density to increase over that of a MLC device at the expense of performance and endurance. The same SLC and MLC principles apply to TLC devices. This is the reason why TLC devices will have the highest density, but the lowest performance and endurance. Typical endurance for a TLC device is rated at about 1k cycles. TLC devices would only be a good fit for low end applications where performance and endurance is not important.

4   Future Trends

As NAND flash memory technologies approach 1X nm process nodes, it will become very difficult to achieve the same performance and endurance of the 3X/2X process node products. Each electron will have a larger impact on a smaller geometry floating gate which makes it even more susceptible to any leakage or disturbs. This is the reason why the RBER will continue to increase as the process shifts to smaller geometry devices and require more error correction. Processors or memory controllers will need to be selected to support these higher error correction requirements. Legacy processors or controllers may not be compatible with the NAND flash products which have higher ECC requirements. Figure 4 shows a trend of ECC requirements across process technology nodes.

Figure 4. SLC and MLC ECC Trend
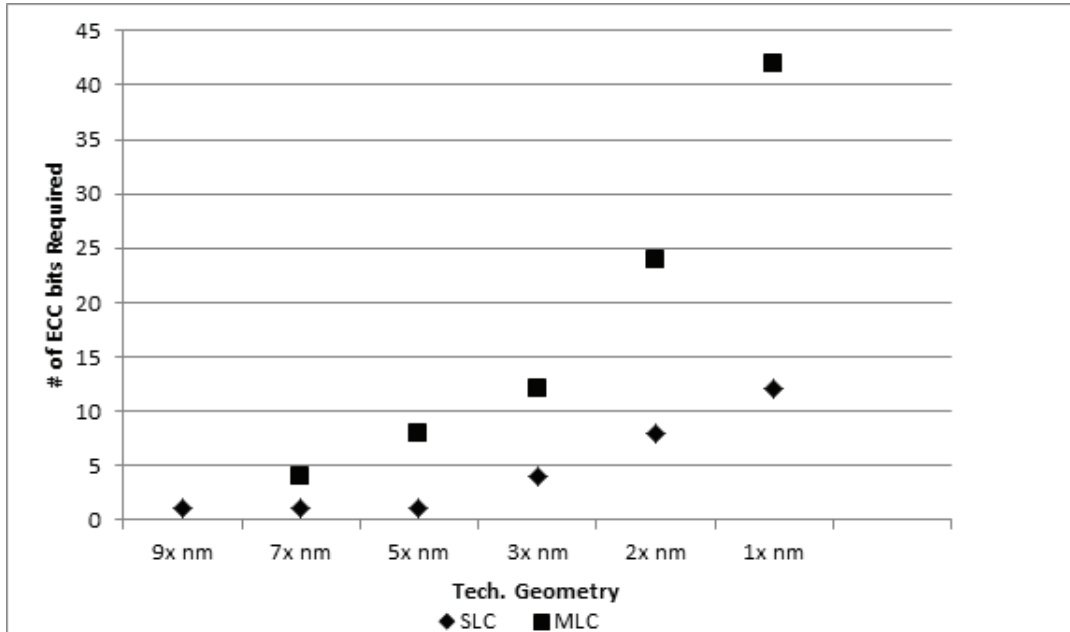
5   Conclusion

Table 2 summarizes the advantages and disadvantages of using a MLC or SLC NAND flash product.

Table 2. Advantages and Disadvantages between SLC and MLC Devices

Feature	SLC	MLC
Higher Density		X
Lowest Cost per Bit		X
Higher Program/Erase Cycles	X	
Lower Error Rate	X	
Program and Erase Speeds	X	
Partial Page Programming	Supported	Not Supported
Copyback Programming	Supported	Not Supported

MLC does have the advantage in higher density and lower cost per bit. This makes it suitable for consumer applications since it has reasonable endurance along with lower costs than SLC. However, SLC will be better suited for applications which require better performance, higher endurance and lower error rates. Such applications would include automotive, communications and industrial products since reliability would be the key factor in choosing which type of NAND memory to use. Due to the significant differences in SLC and MLC NAND

memories, it is important to know the system requirements in order to choose the right type of NAND flash memory to design with. See Table 3.

Table 3. Recommended NAND Memory Type by Application

Application	SLC	MLC
Mobile		X
Computing		X
Consumer		X
Communication/Networking	X	
Industrial	X	
Automotive	X	
Memory Cards		X

Note:

1. This is only a recommendation and the decision on which memory type to choose should be based on the actual usage model.

Document History Page

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*A	5005544	MSWI	11/06/2015	Updated to Cypress template.
*B	5822980	AESATMP8	07/18/2017	Updated logo and Copyright.
*C	6310161	MNAD	09/14/2018	Updated to new template. Completing Sunset Review.
*D		MNAD	06/04/2019	Updated to SkyHigh format.