Recommended PCB Routing Guidelines for S34ML-3 SLC NAND Flash Memory

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Associated Part Families: S34ML-3

AN223194 provides general routing guidelines for PCBs designed with a SkyHigh S34ML SLC NAND flash memory device. This application note is intended for PCD layout designers.

1 Introduction

This application note provides general routing guidelines for PCBs designed with the SkyHigh S34ML-3 NAND flash memory family. Following these guidelines does not eliminate the need to perform signal integrity/power delivery and signal timing/crosstalk simulations using the SkyHigh-provided IBIS models. These guidelines only offer an initial reference towards a PCB design using a SkyHigh S34ML-3 memory device.

If the PCB design cannot meet or beat the recommendations in this application note, you must run detailed simulations to ensure the exceptions do not degrade the desired performance.

This application note applies to the SkyHigh C34ML-3 device family.

2 Signal Descriptions

Table 1 lists the pin description of the S34ML-3 SLC NAND flash memory device.

Table 1. Pin Descriptions

Signal Name	Type	Description
CE#	Input	Chip Enable. CE# LOW selects the device to perform operations based on the NAND bus signal behavior. When CE# is HIGH all other input signals are ignored and outputs are not actively driven.
CLE	Input	Command Latch Enable. This input enables the latching of the I/O inputs into the Command Register on the rising edge of Write Enable (WE#).
ALE	Input	Address Latch Enable. This input enables the latching of the I/O inputs into the Address Register on the rising edge of Write Enable (WE#).
RE#	Input	Read Enable. The RE# input is the serial data-out control, and when LOW drives the data onto the I/O bus. Data is valid t_{REA} after the first falling edge of RE#. Each additional RE# falling edge while CE#, CLE, and ALE remain LOW, increments the internal column address counter by one to deliver the next sequential data output.
WE#	Input	Write Enable. This input latches Command, Address, and Data. The I/O inputs are latched on the rising edge of WE#.
WP#	Input + IPU	Write Protect. The WP# input, when LOW, provides hardware protection of the entire memory address space against undesired data modification (program/erase). This input has a weak internal pull-down (PD) to disable the volatile protection features if the input is left floating.
VPE	Input + IPD	Volatile Protection Enable. The Volatile Protection Enable input, when HIGH during power-on, provides block granularity hardware protection against undesired data modification (program/erase). This input has a week input signal pull-down (IPD) to disable the volatile protection features if the input is left floating.
R/B#	Output, Open Drain	Ready Busy. The Ready/Busy input or output is an Open Drain signal that detects the state of attached memory or signals the state of the controller.
I/O[7, 0]	Input/Output	Inputs/Outputs. The I/O signals are used for command input, address input, data input, and data output. The I/O signals float to HI-Z when the device is deselected or the outputs are disabled.

Table 2 groups the S34ML-3 SLC NAND flash memory signals in the ascending order of signal integrity (SI) priority constraints.

Table 2. Signals Grouping with Signal Integrity (SI) Constraints Priority

Signal Type	Pin Name	Priority
Data	IO15-IO0	SI Constraints Priority 1
Read/Write Control	RE#, WE#	SI Constraints Priority 2
Other Control	ALE, CLE, CE#	SI Constraints Priority 3
Other signals	WP#, RY/BY#, VPE	SI Constraints Priority 4
Power/Ground	VCC, VSS	Refer to section 5

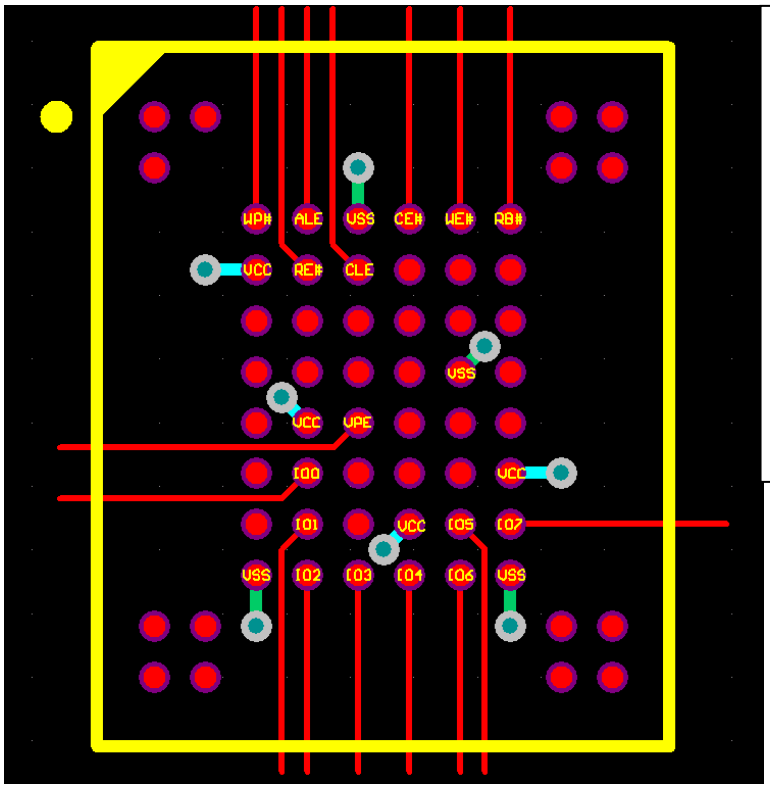
The SI constraints priority does not necessarily mean the routing priority order, but the importance of treating that particular group of signals as high-speed. A common best practice is to route the control signals first and then use datasheet timing relationship between signals to determine the actual trace lengths of other signals.

3 Package Breakout Routing Recommendations

SkyHigh recommends that all signals be broken out on the top layer of the PCB stackup. The power balls/pins (VCC)and ground balls/pins (VSS) can be connected to the nearest power/ground plane through power/ground vias. These vias must be located as close as possible to the S34ML-3 power and ground balls/pins.

Figure 1 shows the 63BGA package PCB breakout recommendation.

Figure 1. FBGA 63 PCB Breakout (Top View, Balls Down)



- Pad size: 0.35 mm (13.78 mils)

- SR (Solder Resist) opening: 0.5 mm (19.69 mils)

- Line width/space: 0.1 mm (4 mils)

- Hole drill size: 0.254 mm (10 mils)

- Via capture pad: 0.495 mm (19.5 mils)

Wide trace for VCC and VSS (width > 20 mils)

All VCC balls can be connected in Bottom Layer using via (for 2-layer PCB).

4 General PCB Signal Routing Guidelines

For simplicity, recommendations in this application note assume a point-to-point routing topology between a memory flash controller and a SkyHigh S34ML-3 NAND flash device. Star or T topologies are not considered in this document. If one of these topologies are used, you must ensure that the appropriate termination resistors are determined based on IBIS simulations. Using NAND FLASH in a daisy-chain topology is not recommended.

The following general guidelines must be considered before and throughout the PCB layout design effort:

- Calculate the impedance of the trace by determining the exact values of signal traces length, width, and trace spacing.
- Use the VSS plane as a primary reference or return path for all signals. Power should only be considered as secondary reference option where a solid continuous ground reference is also present.
- Avoid multiple vias on reference planes to eliminate or minimize return current discontinuity.
- Try to avoid routing signal traces at the edge of the reference plane.
- Route the identified longest signal trace first before routing and adjusting the length of other signal traces.
- Route the same signal groups on the same signal layer and follow the routing from pin to pin as a group (that is, route them together).
- Isolate the ground return path of analog signals from digital signals; i.e., separate digital and analog grounds.
- Use signal integrity tools to estimate the actual trace velocity and path delays to ensure that the assumptions mentioned are not violated.
- Perform signal integrity simulations using SkyHigh-provided IBIS models.

5 Stackup Recommendations

Irrespective of PCB stackups chosen, reference all signal traces to a solid ground plane and dedicate a power plane. The most straightforward stackup to meet this recommendation is a minimum of a 4-layer stackup with the following composition:

- Top Layer (Signal): Add as many GND guard traces next to NAND signals as possible and connect to the GND plane using vias.
- GND
- VCC
- Bottom layer (Signal): Add as many GND guard traces next to NAND signals as possible and connect to GND plane using vias.

It is possible to route S34ML-3 NAND flash in a 2-layer PCB if all signals are properly GND-referenced and VCC trace widths are kept as wide (> 20 mils) as possible.

6 Signal Routing Length, Spacing, and Geometry Constraints

The PCB electrical properties and the recommendations (length, spacing, and geometry constraints) in this application note are based on dielectric material with FR4 assumption. When adjusting signal trace length, a rule of thumb to remember is that routing 1 inch adds a delay of approximately 166 ps. The signal routing lengths are considered from package pin (source) to package pin (destination) by considering the package length compensation while the signal routing spacing between two traces is considered from center to center.

Do the following to achieve a PCB layout with optimal signal integrity and timing margins:

- See the controller and S34ML-3 datasheet timing diagrams to generate AC timing equations for key parameters such as t_{DS}, t_{DH}, t_{CH}, t_{CLH}, t_{REA}, and t_{ALS}.
- **Keep the signal trace impedance around 50 ohms+/-10%.** The Data trace impedance depends on the stackup, and on the trace width and the traces spacing. Based on a 4-layer PCB stackup, this 50-Ω impedance requirement

corresponds to **a trace width of about ~4 to 6 mils and a spacing between traces of about ~3x the trace width (~12 to 18 mils).**

- Determine the signal capacity loading. The absolute maximum total length of signals with respect to their reference plane is defined by the total load capacitance, which directly affects the signal quality.
  - Keep the total load capacitance less than the CLOAD value provided in the datasheet. Allow a margin for
  - spurious/parasitic capacitances that cannot be modeled well.
  - Total load capacitance includes:
    - Total line length capacitance (~3.3 pF/inch with FR4 assumption),
    - Max pin capacitance of controller,
    - Capacitance of any intermediary devices such as connectors and series resistors as well as the parasitic capacitance of connected devices.
- Route the two WE# and RE# Control signals first and determine the length mismatch requirements for Data bus, ALE, and CLE signals based on the datasheet timing relationship (skew) requirement:
  - WE# length determines the length mismatch requirements with I/O through t_{DS}/t_{DH}, ALE through t_{ALS}/t_{ALH}, CE through t_{CH}/t_{CLR}, and CLE through t_{CLHR}.
  - RE# length depends upon the controller access time equation that includes t_{REA}, t_{REH}, and t_{RC}.

  SkyHigh recommends the following length mismatch guidelines:

Signal Group	Length Match Tolerance
Data	+/- 500 mils within the group
WE# to Data	+/- 500 mils
CLE, CLE, ALE to WE	+/- 500 mils
CE to RE# & CLE to RE#	+/- 500 mils

  During the length mismatch analysis, pay attention to signal polarities (rising and falling edge triggers) as well as lead and lag timing to determine whether a specific Control signal should always lead or lag compared to another signal or data bus.
- Route WP#, VPE, and R/B trace to be as short as possible and consider tRR and WP timing.
- Consider the following trace spacing (center-to-center) guidelines to minimize crosstalk effects that can affect signals integrity and delays:
  - Trace spacing within a signal group should be > 3x dielectric height (H) between the signal and ground reference.
  - Trace spacing between signal groups should be > 3x trace width.
  - Trace spacing between NAND signals and other interface signals should be > 3X trace width.

7 Termination

Do the following to ensure a proper termination on NAND flash signal traces:

- Review the drive strength and impedance required for the NAND controller I/O and the transmission line routing load to determine whether series terminations are needed. The drive strength can easily be determined by looking at the IBIS IV/VT curves for the three PVT corners (typical, min and max).
- Add pull-up resistor on the R/B# signal trace (see the datasheet for the exact value).

8 Power Delivery Guidelines

Do the following to ensure a proper routing power delivery on NAND flash VCC and VSS signal traces:

- Connect VSS balls/pins to the ground plane. Connect each VSS ball/pins to the internal GND plane with its own unique via to minimize IR drop.

- Connect VCC balls/pins to a single supply plane. Connect each VCC ball/pins to the internal supply plane with its own unique via to minimize IR drop. If a 2-layer PCB is used, all VCC vias must be connected as close to the NAND package as possible with thick traces.
- Where possible, keep at least a 20-mil gap between power planes.
- If possible, provide at least an 80-mil gap between power islands on the same layer.
- VCC islands must be large enough and not have “bottle necks.” The power island must be at least 250-mils wide at the narrowest area.
- Except in the package breakout area, maintain a minimum trace width of 20 mils for all supply traces. Both supply and ground traces (or planes) must be closely coupled to each other (i.e., route them close to each other to avoid large inductive loops).
- Keep supply trace lengths ≦ 400 mils and tracing width ≧ 20 mils.
- Maintain low-impedance routing (traces >20 mils) from voltage regulator to flash supply pins as well as from voltage regulator to the controller flash supply pins.
- If the voltage regulator is not on the same PCB as the flash packages (modularization), aim to the reach the lowest impedance on VCC/VSS routing (for example, wider traces).
- If the controller main board and memory module are not on the same board, it is recommended to use a *G: S/P: G* type of connector configuration where S refers to signal, G refers to GND, and P refers to VCC.
- Add VCC/GND test points close to each flash package as well as next to voltage regulator module (VRM). This allows the measurement of the VCC-GND waveform at both VRM as well as flash packages.
- Add decoupling capacitors per the following recommendations:
  - Place PCB decoupling capacitors as close to the package as possible.
  - Place at least two 1-µF 0402 ceramic capacitors near each side of the package.
  - Ensure that these capacitors have low ESL (Equivalent Series Inductance) and ESR (Equivalent Series Resistance).
  - Keep the VCC and GND trace routing from the capacitor as wide as possible to avoid inductive/resistive effects.
  - In addition to the decoupling capacitors, place two 0.1-µF 0402 ceramic capacitors as close to the package as possible.
  - Use X7R or X5R ceramic capacitors with the rated voltage greater than or equal to twice VCC max.

9 Test Points and Oscilloscope Measurements

Test points are often added on the PCB to make some measurements or probing some signals. Here are the recommendations on where and how to place these test points:

- For IO0-15 and R/B# signals, add test points close to controller and S34ML-3 NAND flash. For other signals, add test points close to the S34ML-3 NAND Flash memory package.
- When the memory controller is driving, probe the signals as close as possible to the NAND flash. When the NAND flash is driving, probe the signals as close as possible to memory controller.
- While creating a test pad, the stub (extra inductance and capacitance) resulting from such pad should be minimized. Probing at the break-out via is better than creating test pad stubs. In the case of a 4-layer PCB with through-hole vias, if possible, probe the signals at the bottom of the PCB on these vias.
- While performing scope measurements, use a 3-GHz or greater bandwidth scope and low-impedance probes to see the waveform transition (such as rising and falling portion of the waveform) more accurately.
- Always measure VCC-VSS at the controller, voltage regulator, or next to the connector (either side) and at flash. This needs to be done before making any signal measurements to ensure that the supply is not noisy. A noisy supply impacts signal timing. In addition, these measurements establish the IR drop from regulator to controller OR regulator to flash.
- While measuring signals, it is a good idea to set the trigger on the most common switching signals such as WE#.

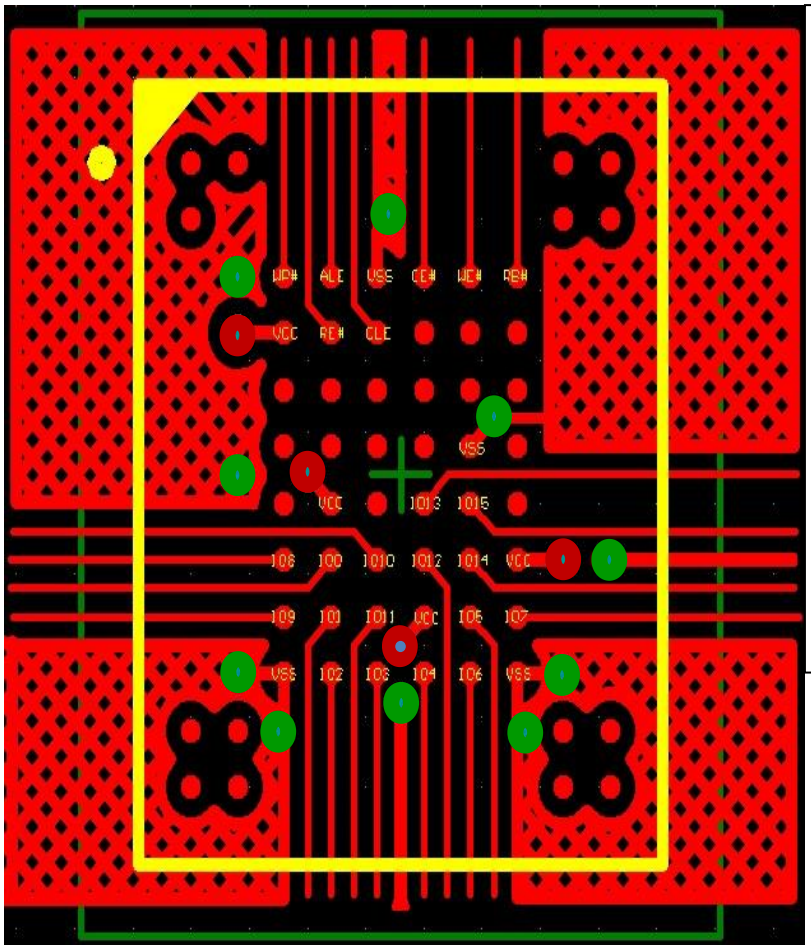
10 NAND Packages Layout Examples

Figure 2 to Figure 4 provide the recommendations of 4-layered PWB design, including pad and SR opening size, trace width/space, via capture pad and hole drill size, as well as the recommended escape routing and VCC/VSS plane and its location.

These breakout examples are recommendations. Since every customer has different PCB stackup/component placements, you should weigh those factors prior to using these recommendations.

For more details, see *Escape Routing for NAND Packages.pdf* available with this application note.

Figure 2. 63-BGA, x8 Device Breakout (Top View, Balls Down)



Pad size: 0.35 mm (13.78 mil)

SR opening: 0.5 mm (19.69 mil)

Line width/space: 0.1 mm (4 mil)

(Trace width for VCC and VSS should be as wide as possible)

Hole drill size: 0.254mm (10 mil)

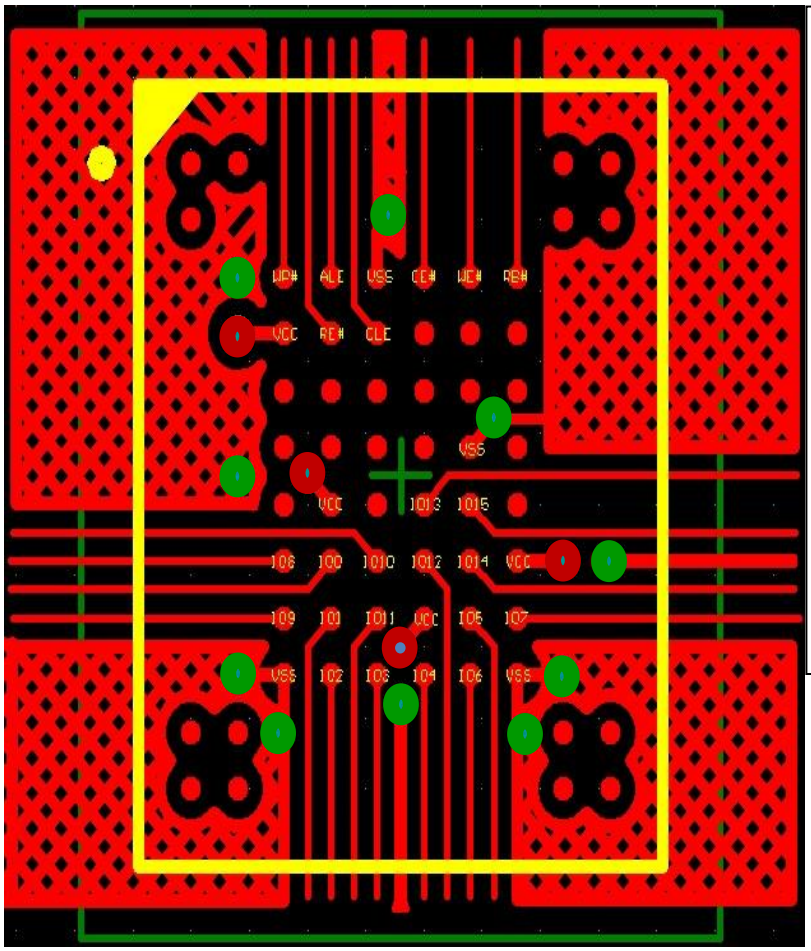
Via capture pad: 0.495mm (19.5 mil)

VCC can be connected to VCC Plane in the third layer using VCC via

VSS can be connected to the GND plane in the second and fourth layer using VSS via

VSS plane in the top layer is used to shield signal traces and placed next to VCC via

Figure 3. 63-BGA, x16 Device Breakout (Top View, Balls Down)



Pad size: 0.35 mm (13.78 mil)

SR opening: 0.5 mm (19.69 mil)

Line width/space: 0.1 mm (4 mil)

(Trace width for VCC and VSS should be as wide as possible)

Hole drill size: 0.254 mm (10 mil)

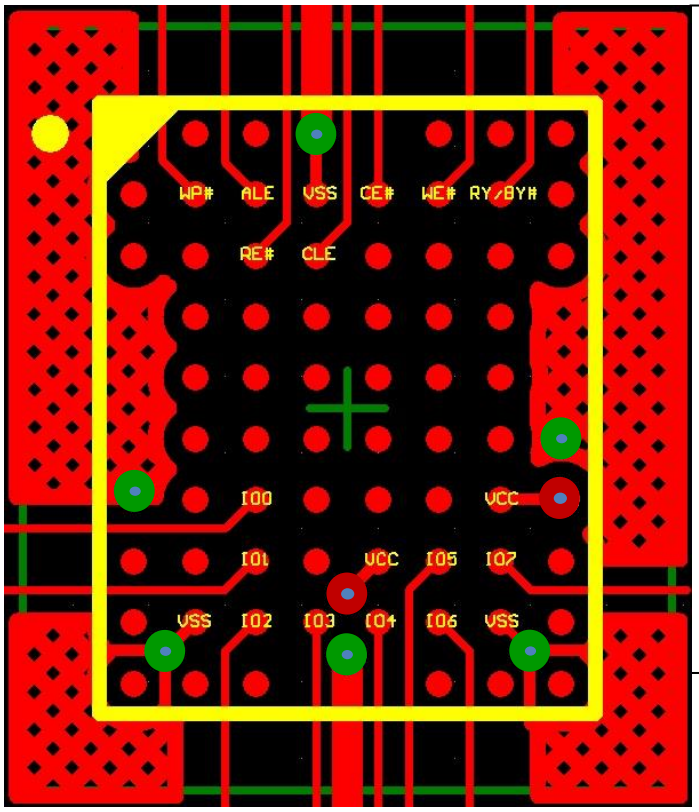
Via capture pad: 0.495 mm (19.5 mil)

VCC can be connected to VCC Plane in the third layer using VCC via

VSS can be connected to the GND plane in the second and fourth layer using VSS via

VSS plane in the top layer is used to shield signal traces and placed next to VCC via

Figure 4. 63-BGA, x16 Device Breakout (Top View, Balls Down)



Pad size: 0.35 mm (13.78 mil)

SR opening: 0.5 mm (19.69 mil)

Line width/space: 0.1 mm (4 mil)

(Trace width for VCC and VSS should be as wide as possible)

Hole drill size: 0.254 mm (10 mil)

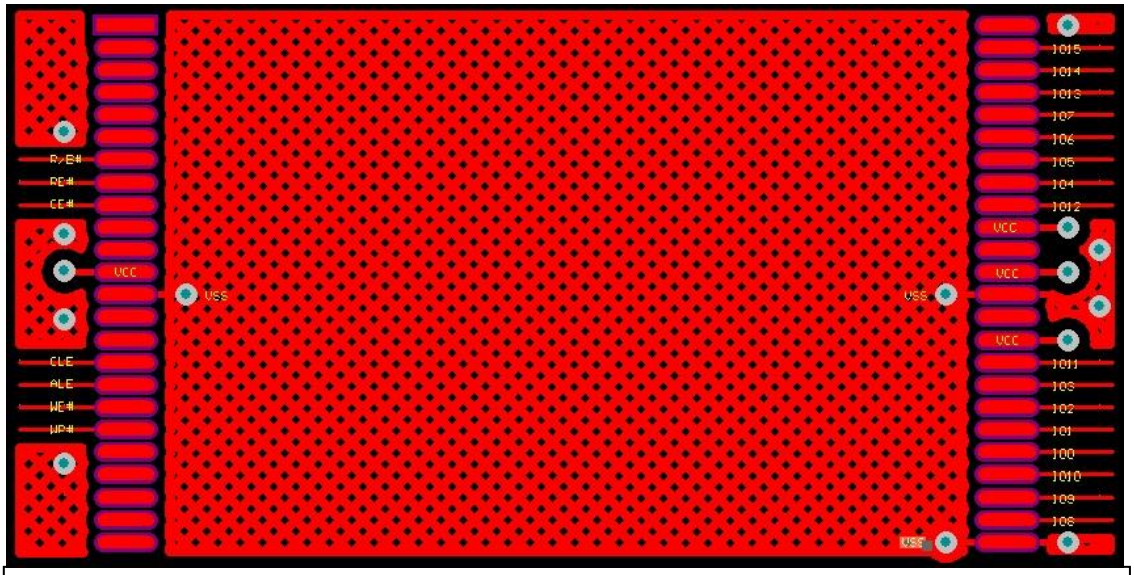
Via capture pad: 0.495 mm (19.5 mil)

VCC can be connected to VCC Plane in the third layer using VCC via

VSS can be connected to the GND plane in the second and fourth layer using VSS via

VSS plane in the top layer is used to shield signal traces and placed next to VCC via

Figure 5. 48-TSOP1, x16 Device Breakout (Top View, Balls Down)



Pad size: 1.3 x 0.3 mm (51.18 x 11.8 mil)

SR opening: 0.075 mm clearance between the edge of the pad and solder mask

Line width/space: 0.1 mm (4 mil)

(Trace with for VCC and VSS should be as wide as possible)

Hole drill size: 0.254 mm (10 mil)

Via capture pad: 0.495 mm (19.5 mil)

VCC can be connected to VCC Plane in the 3rd layer using VCC via

VSS can be connected to the GND plane in the 2nd and 4th layer using VSS via

VSS plane on the top layer is used to shield signal traces and placed next to VCC via

11 Conclusion

This application note provides general routing guidelines for PCBs designed with a S34ML-3 Flash memory device. For any questions regarding this application note, go to www.skyhighmemory.com or contact your SkyHigh Memory representative.

12 Related Documents

Datasheets:

- 002-19204 - S34ML04G3, 4 GB, 3 V, 2K PAGE SIZE, x8 I/O, SLC NAND FLASH MEMORY FOR EMBEDDED (ADVANCE)
- 002-19822 - S34ML04G3, 4 GB, 3 V, 4K PAGE SIZE, x8 I/O, SLC NAND FLASH MEMORY FOR EMBEDDED (ADVANCE)

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*A		MNAD	05/02/2019	updated to SkyHigh format