1.1. **S34ML-1 Product 48 nm**

SLC NAND

48 nm SLC NAND was introduced in July 2012 and utilize tunnel Oxide, Polysilicon floating gate and interconnections are three metal layers with contact plugs and barrier metals. The 1st Metal layer for 48 nm SLC NAND is using Tungsten.

Data Summary and Failure Rate Estimation using Exponential Model HTOL Stress Temperature - 125°C

		int / Test sult	Modeling Parameters @ 55°C					Average F	Average Failure Rate	
Failure Mechanisms	Early Life (hrs)	Inherent Life (hrs)	Ea eV	TAF	VAF	OAF	MTTF (yrs)	Early Life (PPM)	Inherent Life (FITS)	
	96	1000					(313)	(1.1.111)	(1110)	
Sample Size	2810	900								
125C, Zero fails, Process ave. Ea	0	0	0.7	74	1	74		0	14	
							8317			

Data Retention Bake - 150°C

Reliability Stress	Sample Size	Reject	PPM	FITS
500	77	0	0	2
1000	693	0	0	2



1.2. S34ML-1 Product Families

41 nm SLC NAND

41 nm SLC NAND were introduced in Jun 2012 and utilize tunnel Oxide, Polysilicon floating gate and interconnections are three metal layers with contact plugs and barrier metals. The 1st Metal layer for 41 nm SLC NAND is using Copper.

Data Summary and Failure Rate Estimation using Exponential Model HTOL Stress Temperature - 125°C

		nd Point / Test Result Modeling Parameters @ 55°C					Average Failure Rate		
Failure Mechanisms	Early Life (hrs)	Inherent Life (hrs)	Ea eV	TAF	VAF	OAF	MTTF (yrs)	Early Life (PPM)	Inherent Life (FITS)
	96	1000					(313)	(1.1.111)	(1110)
Sample Size	3000	1002							
125C, Zero fails, Process ave. Ea	0	0	0.7	74	1	74		0	12
							9259		

Data Retention Bake - 150°C

Reliability Stress	Sample Size	Reject	PPM	FITS
500	154	0	0	
1000	692	0	0	1
2000	77	0	0	



1.3. S34ML-2 Product

Families 32 nm SLC

NAND

32 nm SLC NAND were introduced in October 2012 and utilize tunnel Oxide, Polysilicon floating gate and interconnections are three metal layers with contact plugs and barrier metals. The 1st Metal layer for 32 nm SLC NAND is using Copper

Data Summary and Failure Rate Estimation using Exponential Model HTOL Stress Temperature - 125°C

	Read Po Res	int / Test sult	Model			ling Parameters @ 55°C			Average Failure Rate	
Failure Mechanisms	Early Life (hrs)	Inherent Life (hrs)	Ea eV		TAF	VAF	OAF	MTTF (yrs)	Early Life (PPM)	Inherent Life (FITS)
	96	1000						(3.5)	()	(1110)
Sample Size	3000	1320								
125C, Zero fails, Process ave. Ea	0	0	0.7		74	1	74		0	9
									U	9
								12198		

Data Retention Bake - 150°C

Reliability Stress	Sample Size	Reject	PPM	FITS
500	231	0	0	
1000	923	0	0	

2. Data Summaries by Package Family

2.1. BGA (Ball Grid Array)

Reliability Stress		Sample Size	Reject	Failure Rate PPM
HAST	96hrs	1666	0	0
	264hrs	2577	0	0
HIGH TEMP STORAGE	1000hrs	5435	0	0
TEMP CYCLE	500cycle	3072	0	0
	1000cycle	3586	0	0
UNBIASED HAST TEST	96hrs	4723	0	0
	264hrs	635	0	0

2.2. TSOP (Thin Small Outline Package)

Reliability Stress		Sample Size	Reject	Failure Rate PPM
HAST	96hrs	4211	0	0
	264hrs	100	0	0
HIGH TEMP STORAGE	1000hrs	5025	0	0
PRESSURE COOKER TEST	96hrs	480	0	0
	168hrs	2507	0	0
TEMP CYCLE	500cycle	6161	0	0
	1000cycle	316	0	0
UNBIASED HAST TEST	96hrs	2688	0	0

